## Listing and Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) Method for the management of data received via a serial data bus, comprising the steps of:

[[the data being]] receiving data transmitted in bus packets having a variable length, the data being divided into data blocks having a defined length, a combination of a defined number n of data blocks forming a data source packet, section-by-section transmission of the data source packet within the framework of data blocks being permitted [[, wherein]] ; and

carrying out a modulo-n counting of the data blocks [[is carried out]] in order to determine the data source packet boundaries, and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval.

2. (Currently Amended) Method according to Claim 1, wherein each bus packet is subjected to CRC checking and the checking results are buffer-stored in order to be able to ascertain whether a data source packet transmitted in two or more bus packets has been transmitted without [[any]] transmission errors.

3. (Previously Presented) Method according to Claim 1 wherein a reference counter reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data blocks is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal is output in the event of non-correspondence.

4. (Previously Presented) Method according to Claim 1, wherein the defined number n of data blocks of a data source packet corresponds to the number 8 and the modulo-n counting is correspondingly modulo-8 counting.

5. (Previously Presented) Apparatus for carrying out the method according to Claim 1, having a memory unit to which the received data are written in order, and having a memory management device wherein a modulo-n counter is provided, which counts the received data blocks and outputs a data source packet start signal to the memory management device at the beginning of the next counting interval.

6. (Previously Presented) Apparatus according to Claim 5, further comprising a CRC checking unit, by means of which the data in the received bus packets are checked with regard to freedom from errors, where the checking results of a plurality of successive bus packets are buffer-stored and combined if the data source packet start signal has been identified, and where the CRC checking unit outputs an error signal if one of the combined checking results includes an identified error.

7. (Previously Presented) Apparatus according to Claim 5, further comprising a data block reference counter, which effects the comparison counting of the received data blocks, and where comparison means are provided which compare the counter reading of the data block reference counter with the received reference counter reading of the bus packet and output an error signal in the event of non-correspondence.

8. (Previously Presented) Apparatus according to Claim 1, further comprising a data counter, by which the data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been counted are as many as are defined as belonging to a data block.

9. (Previously Presented) Apparatus according to Claim 1, wherein the data bus is designed according to the IEEE 1394 standard and the apparatus is part of a data link layer module in the interface for this data bus.